

Figure 1: Chip Micrograph

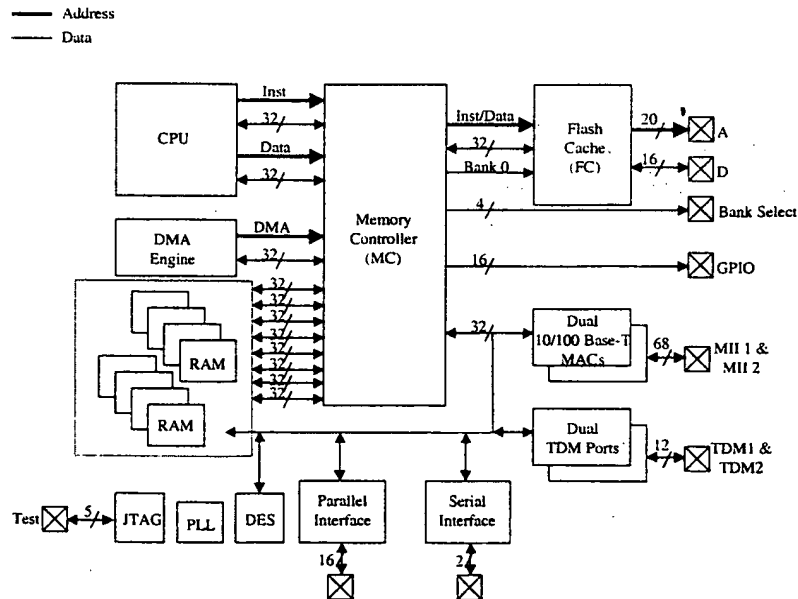
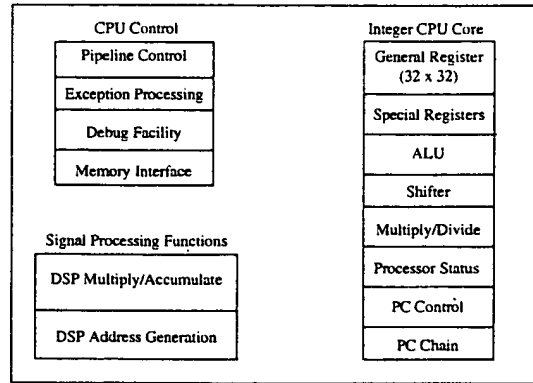


Figure 2: Processor Block Diagram



Pipeline: IF RF EXE MEM WB

IF: Instruction Fetch, RF: Register Fetch, EXE: Execute, MEM: Memory Access, WB: WriteBack

Figure 3: CPU Architecture and Pipeline

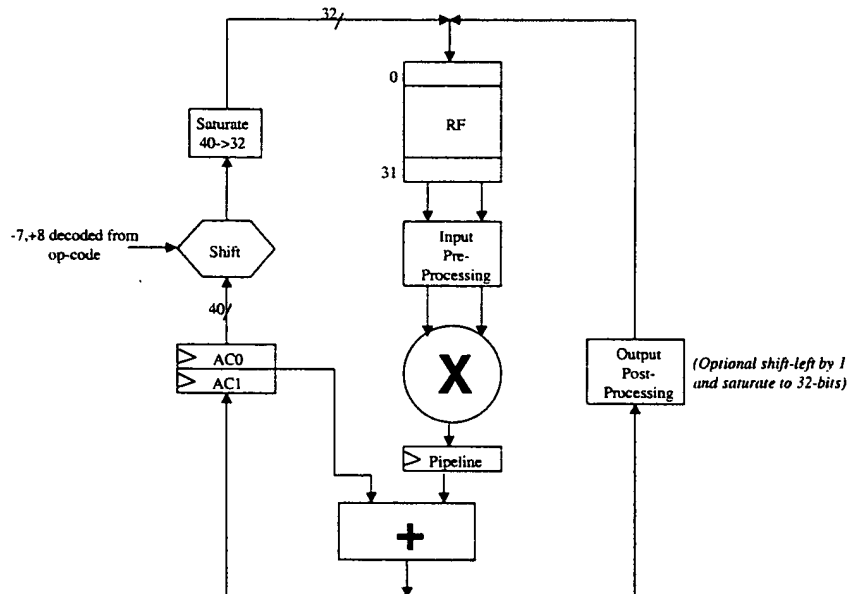


Figure 4: DSP Multiply-Accumulate Unit

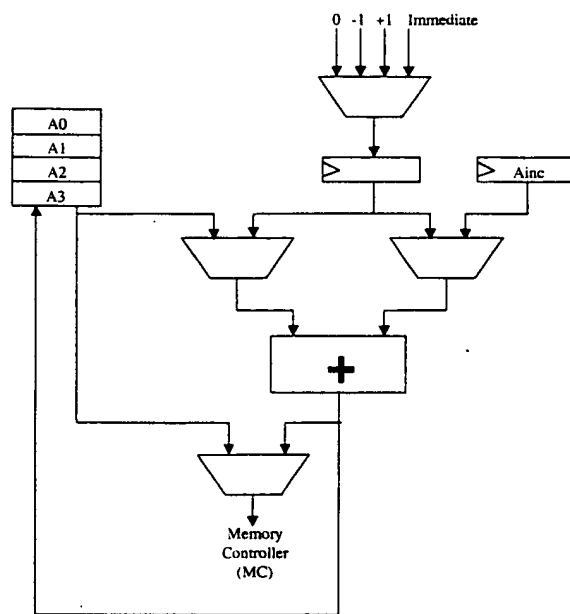


Figure 5: DSP Address Generation Unit

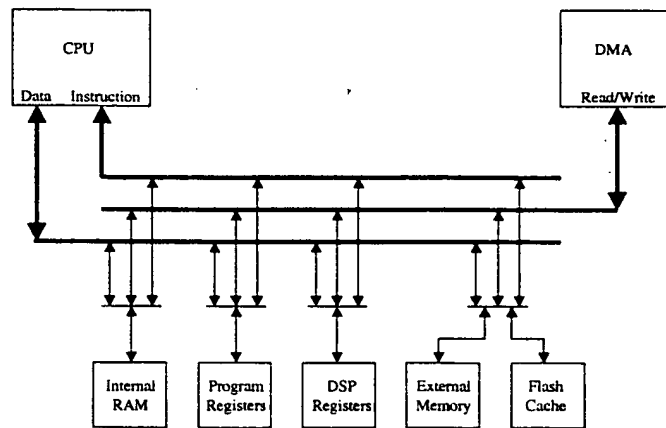


Figure 6: Memory Controller Crosspoint Switch

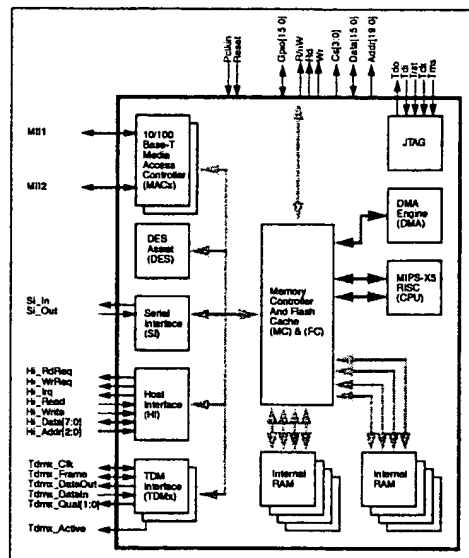


Figure 7: Terminal Processor Architecture Summary

- MIPS-X5 Combined RISC and DSP core (200+ DSP MIPS).
- 256KBytes on chip RAM, 8 way interleaved, with single cycle access. 64 Bytes of boot ROM.
- Two 10/100 Base - T Ethernet MACs with MII interface.
- 8 KByte, 2 way set associative cache for external flash program memory.
- Glueless support of SLIC/SLAC codecs and character LCD displays via TDM & GPIO ports.
- GCC based compiler support with assembler and debugger.
- Low power. 1.8V +/- 10% core voltage, 3.3V +/- 10% I/O voltage.
- 176 TQFP package/JTAG.

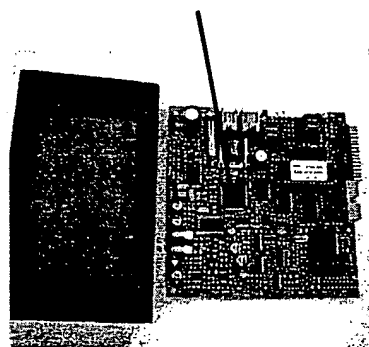
- Software Development Tools
 - Dynamic linker, boot mechanism, compiler test suite, gdb/debug
- POSIX Operating System
 - Interrupt vector, context switching method, scheduling, semaphores, CLIB/printf
- Device Drivers
 - MAC, TDM, Host, UART
- Audio Libraries
 - G.711, G.723, G.729A, G.729E, Acoustic Echo Cancellation
- Managers
 - Audio, MAC/Network
- Applications
 - Audio loopback
 - MGCP/H.323 loopback

Figure 8: Terminal Processor Software Co-Development Tasks

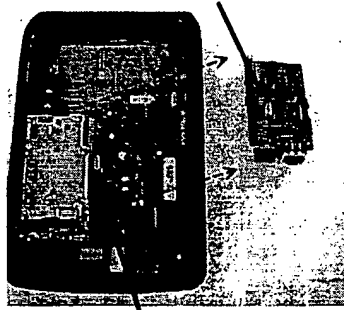
- 8x8's implementation of the POSIX operating system.
- Full support for:
 - Threads (single process, multiple threads)
 - Scheduling (two algorithms -- FIFO and round robin)
 - Semaphores
 - Mutexes
 - Condition Variables
 - Message Queues
 - Signals and Timers

Figure 9: Terminal Processor Embedded OS Features

Modern Digital PBX Phone



**Terminal Processor
IP Telephony Module**



**IP-enabled PBX
Phone Terminal**

Figure 10: Terminal Processor Reference Design

